**WHAT IS CLAIMED IS:**

1. A semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of first and second word lines arranged in the rows; and

a plurality of first and second bit lines arranged in the columns, wherein

each of the plurality of memory cells includes a first transistor, a second transistor and a capacitor,

the first transistor is connected between a corresponding first bit line and the capacitor and receives a voltage on a corresponding first word line at its gate, and

the second transistor is connected between a corresponding second bit line and the capacitor and receives a voltage on a corresponding second word line at its gate,

the semiconductor memory device further comprising:

a data line;

a plurality of first column selection switches provided corresponding to the plurality of first bit lines, and each connecting and disconnecting a corresponding first bit line to and from the data line;

a plurality of second column selection switches provided corresponding to the plurality of second bit lines, and each connecting and disconnecting a corresponding second bit line to and from the data line;

a word line driver for driving first and second word lines corresponding to a memory cell to be accessed;

a column selection circuit for turning ON/OFF first and second column selection switches corresponding to the memory cell to be accessed;

an input/output (I/O) buffer for receiving and outputting data from and to the outside; and

a data transfer circuit for transferring data read from a memory cell to the data line to the I/O buffer and transferring write data from the I/O buffer to the data line, wherein

the word line driver and the column selection circuit conduct interleave operation, and the data transfer circuit and the I/O buffer do not conduct interleave operation.

2. The semiconductor memory device according to claim 1, wherein

the data line includes a write data line and a read data line, and

each of the plurality of first and second column selection switches connects and disconnects a corresponding bit line to and from the write data line in order to write data to a memory cell, and connects and disconnects the corresponding bit line to and from the read data line in order to read data from a memory cell.

3. The semiconductor memory device according to claim 1, wherein the data line is a single-type data line.

4. A semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of first and second word lines arranged in the rows; and

a plurality of first and second bit lines arranged in the columns, wherein

each of the plurality of memory cells includes a first transistor, a second transistor and a capacitor,

the first transistor is connected between a corresponding first bit line and the capacitor and receives a voltage on a corresponding first word line at its gate, and

the second transistor is connected between a corresponding second bit line and the capacitor and receives a voltage on a corresponding second word line at its gate,

the semiconductor memory device further comprising:

a first data line;

a second data line;

a plurality of first column selection switches provided corresponding to the plurality of first bit lines, and each connecting and disconnecting a corresponding first bit line to and from the first data line;

a plurality of second column selection switches provided corresponding to the plurality of second bit lines, and each connecting and disconnecting a corresponding second bit line to and from the second data line;

a word line driver for driving first and second word lines corresponding to a memory cell to be accessed;

a column selection circuit for turning ON/OFF first and second column selection switches corresponding to the memory cell to be accessed;

an input/output (I/O) buffer for receiving and outputting data from and to the outside;

a data transfer circuit; and

a switching means for transferring data read from a memory cell to the first or second data line to the data transfer circuit and transferring the data from the data transfer circuit to the first or second data line, wherein

the data transfer circuit transfers data from the switching means to the I/O buffer and transfers data from the I/O buffer to the switching means, and

the word line driver, the column selection circuit and the switching means conduct interleave operation, and the data transfer circuit and the I/O buffer do not conduct interleave operation.

5. The semiconductor memory device according to claim 4, further comprising:

a read data line for transferring data from the switching means to the I/O buffer; and

a write data line for transferring data from the I/O buffer to the switching means.

6. A semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of word lines arranged in the rows;

a plurality of bit line pairs arranged in the columns;

a data line pair;

a decoder for generating an active signal when data is written to any of the plurality of memory cells;

a write circuit responsive to the active signal from the decoder, for activating one or the other data line of the data line pair according to write data;

a plurality of first transistors connected between one data line of the data line pair and one bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on the one data line of the data line pair;

a plurality of second transistors connected between the other data line of the data line pair and the other bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on the other data line of the data line pair;

a plurality of third transistors connected between the plurality of first transistors and one bit lines of the plurality of bit line pairs;

a plurality of fourth transistors connected between the plurality of second transistors and the other bit lines of the plurality of bit line pairs; and

a column selection circuit for applying an active signal to a gate of one of the plurality of third transistors which corresponds to a bit line pair corresponding to a memory

cell to be written and for applying an active signal to a gate of one of the fourth transistors which corresponds to the bit line pair.

7. The semiconductor memory device according to claim 6, wherein

the plurality of first transistors are turned ON/OFF in response to a voltage on the other data line of the data line pair instead of the voltage on the one data line of the data line pair, and

the plurality of second transistors are turned ON/OFF in response to a voltage on the one data line of the data line pair instead of the voltage on the other data line of the data line pair.

8. The semiconductor memory device according to claim 6, wherein the first and second transistors are CMOS (Complementary Metal Oxide Semiconductor) transistors.

9. The semiconductor memory device according to claim 6, further comprising:

a sense amplifier for amplifying a potential difference of a bit line pair corresponding to a memory cell to be written after the bit line pair is driven according to write data.

10. The semiconductor memory device according to claim 9, further comprising:

a precharge circuit for precharging a bit line pair corresponding to a memory cell to be written for a predetermined period after the bit line pair is driven according to write data until the sense amplifier amplifies a potential difference of the bit line pair.

11. A semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of word lines arranged in the rows;

a plurality of bit line pairs arranged in the columns;

a data line pair;

a decoder for generating an active signal when data is written to any of the plurality of memory cells;

a write circuit responsive to the active signal from the decoder, for activating one or the other data line of the data line pair according to write data;

a plurality of first transistors connected between a node receiving a power supply voltage or a ground voltage and one bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on one data line of the data line pair;

a plurality of second transistors connected between the node and the other bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on the other data line of the data line pair;

a plurality of third transistors connected between the plurality of first transistors and one bit lines of the plurality of bit line pairs;

a plurality of fourth transistors connected between the plurality of second transistors and the other bit lines of the plurality of bit line pairs; and

a column selection circuit for applying an active signal to a gate of one of the plurality of third transistors which corresponds to a bit line pair corresponding to a memory cell to be written and for applying an active signal to a gate of one of the plurality of fourth transistors which corresponds to the bit line pair.

12. The semiconductor memory device according to claim 11, wherein the first and second transistors are CMOS transistors.

13. The semiconductor memory device according to claim 11, further comprising:

a sense amplifier for amplifying a potential difference of a bit line pair corresponding to a memory cell to be written after the bit line pair is driven according to write data.

14. The semiconductor memory device according to claim 13, further comprising:

a precharge circuit for precharging a bit line pair corresponding to a memory cell to be written for a predetermined period after the bit line pair is driven according to write data until the sense amplifier amplifies a potential difference of the bit line pair.

15. A semiconductor memory device, comprising:

a first main amplifier activated in response to an active first enable signal, for amplifying data read from a first memory cell;

a first tri-state buffer for driving an output node of the first tri-state buffer according to the data amplified by the first main amplifier when the first enable signal is active, and rendering the output node in a high impedance state when the first enable signal is inactive; and

a first latch circuit for latching and outputting data of the output node of the first tri-state buffer to the outside.

16. The semiconductor memory device according to claim 15, further comprising:

a second latch circuit; and

a switch connected between the output node of the tri-state buffer and the second latch circuit, for connecting the output node of the tri-state buffer to the second latch circuit

in a test mode, and disconnecting the output node of the tri-state buffer from the second latch circuit in a normal mode.

17. The semiconductor memory device according to claim 16, wherein either the first or second latch circuit that is not used is not allowed to conduct latch operation.

18. The semiconductor memory device according to claim 15, further comprising:

a second main amplifier activated in response to an active second enable signal, for amplifying data read from a second memory cell;

a second tri-state buffer for driving an output node of the second tri-state buffer according to the data amplified by the second main amplifier when the second enable signal is active, and rendering the output node in a high impedance state when the second enable signal is inactive;

a second latch circuit for latching and outputting data of the output node of the second tri-state buffer to the outside; and

a switch connected between an output node of the first latch circuit and an output node of the second latch circuit, and turned ON/OFF according to a bit width of read data.

19. The semiconductor memory device according to claim 18, wherein either the first or second latch circuit that is not used is not allowed to conduct latch operation.

20. A semiconductor memory device, comprising:

an output buffer for outputting data read from a memory cell to an output terminal, wherein

the output buffer includes

a first buffer for driving the output terminal according to the data read from the memory cell, and

a second buffer having an active state and an inactive state, for driving the output terminal according to the read data in the active state.

21. The semiconductor memory device according to claim 20, wherein the second buffer is activated and inactivated according to a bit width of the data read from the memory cell.

22. The semiconductor memory device according to claim 21, wherein the second buffer is activated and inactivated according an external signal capable of recognizing the bit width of the data read from the memory cell.

23. The semiconductor memory device according to claim 21, wherein the second buffer is activated and inactivated by using a fuse element representing the bit width of the data read from the memory cell.

24. The semiconductor memory device according to claim 20, further comprising:

a detector for detecting an operating frequency of the semiconductor memory device, wherein

the second buffer is activated and inactivated according to the operating frequency detected by the detector.

25. A semiconductor memory device, comprising:

a plurality of memory cells arranged in rows and columns;

a plurality of word lines arranged in the rows;

a plurality of bit line pairs arranged in the columns;

a data line pair;

a plurality of first transistors connected between a node receiving a first voltage and one bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on one data line of the data line pair;

a plurality of second transistors connected between the node and the other bit lines of the plurality of bit line pairs, and turned ON/OFF in response to a voltage on the other data line of the data line pair;

a plurality of third transistors connected between the plurality of first transistors and one bit lines of the plurality of bit line pairs;

a plurality of fourth transistors connected between the plurality of second transistors and the other bit lines of the plurality of bit line pairs;

a column selection circuit for applying an active signal to a gate of one of the plurality of third transistors which corresponds to a bit line pair corresponding to a memory cell to be written and for applying an active signal to a gate of one of the plurality of fourth transistors which corresponds to the bit line pair; and

a write circuit for activating one or the other data line of the data line pair according to write data and a level of the first voltage received by the node when data is written to any of the plurality of memory cells.

26. The semiconductor memory device according to claim 25, further comprising:

a means for supplying a power supply voltage or a ground voltage to the node as the first voltage according to an address specifying the plurality of memory cells.

27. The semiconductor memory device according to claim 25, further comprising:

a means for supplying a power supply voltage or a ground voltage to the node as the first voltage according to an operating frequency of the semiconductor memory device.

28. The semiconductor memory device according to claim 25, further comprising:

a means for supplying a power supply voltage or a ground voltage to the node as the first voltage according to a precharge potential of one of the plurality of bit line pairs.

29. The semiconductor memory device according to claim 25, further comprising:

a means for supplying a power supply voltage or a ground voltage to the node as the first voltage according to external control.